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(54) **Scene tracker system.**

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Scene Tracker System

The present invention relates to a tracker system for scanning a scene in a field of view and comprising, a scanner, means responsive to the scanner for producing digital data signals for defining the scene, and reference data signal storage and correlator circuits for comparing reference data signals and live data signals, the latter resulting from a subsequent scan of the scene.

Such a tracker system is commonly used with imaging or quasi-imaging sensors such as T.V. cameras, FLIRS, millimeter-wave scanners, or the like and provides a powerful means for updating information in a guidance system.

Systems are known which perform position updating of guidance systems automatically. Such systems typically consist of an imaging sensor which views the ground, one or more reference maps contained in a suitable storage medium, and a computer which compares the images and does the information processing. When the guidance system indicates the vehicle is near the update point, the computer attempts to match the sensor image to the reference image. When a match occurs, the computer establishes a geometric correspondence between reference image points and sensor image points. Then, given a reference image update point, the corresponding sensor image point is determined. This information, with a sensor pointing direction relative to the vehicle body and vehicle altitude, allows computation of the vehicle position and updating of the guidance system. Such an automatic image matching process is commonly implemented by some form of cross-correlation, which is a powerful and practical approach, and one that is optimum under fairly general conditions. The peak of the correlation function is taken as a point of best match between the reference and sensor images.

One of the more important design parameters of image correlators is the correlation area. That is, the integration area used in computing each value of the correlation function. Correlation performance generally improves as the correlation area increases. However, large correlation areas also cause rapid performance loss with geometric distortion between the two images. Geometric distortion arises from different viewing positions for the reference and sensor images, and is a real effect with which most systems must deal. For a given application, it is possible to perform tradeoffs and arrive at an optimum correlation area, but even the resulting optimum performance may be inadequate.

Various methods for achieving cross-correlation between images exist. One such system is represented in French Patent 2,339,869 which, responding to the thermal intensity or the optical brilliance of a scene, generates signals which are stored and compared with live signals from a subsequent scan using the technique of multiplying the magnitudes of pixels of the scene in the stored memory with magnitudes of pixels in corresponding positions in the live data memory resulting from subsequent scans from which the coordinates of the position of the subsequently scanned scene, with respect to the storage scene, are derived. This approach involves a comparatively large correlation area in which problems of distortion, as discussed above, may be involved.

Another approach involving a signal correlation for an entire scene is described in U.S. Patent 3,805,261. Here, a process for controlling the course of a body in motion by comparison of a known relief plot of a surveyed zone with a sounding plot using a radio altimeter, is discussed. The technique described comprises storing a plurality of patterns of binary digits wherein each of the patterns corresponds to a different and known strip of its own. The stored binary digits are representative of the algebraic sign of the difference in heights between predetermined points of the strip. An analog-to-digital converter is used to translate the output of the radio altimeter into a pattern of binary digits representative of the algebraic sign of the difference between readings taken in space conformity with predetermined points. Thereafter, a correlation of the translated pattern with each of the stored patterns of binary digits indicates the degree of correspondence between the path being flown and that of one of the stored paths. As in the system of the French patent briefly discussed above, a multiplier is employed in the correlator. Here, also, there is but a single correlation function for the entire scene.

U.S. Patent 3,943,277, while using a different approach than either of the two patents discussed above, also describes an arrangement in which a single correlation function for the entire scene is derived. Here a correlation function for deriving the Y error signal is obtained using a line-by-line comparison of the digitized video and the X correlation function from which the X error signal is derived is obtained on an element-by-element comparison of the digitized signal. This system employs a shift register for propagating the line and digit signals and a comparator, such as gates, for comparing line and element data both before and after the present element, with integrator for the X and Y coordinates processing the line and element comparisons.

According to the present invention we provide a tracker system characterised by, circuits for producing search cell data signals from a pre-selected plurality of portions of the data signals for one scene, and for storing search cell signals from one scan as reference search cell signals; digital correlation circuits for comparing search cell signals from a subsequent scanning operation with corresponding reference cell signals, on a bit-by-bit basis, and for summing the result of predetermined relationships of said bits, for producing pluralities of correlation sum signal groups, one group for each search and reference cell comparison; digital coordinate circuits for providing pluralities of correlation coordinate signal groups, one coordinate signal group for each cell, individually indicative of the relative position within each search cell of a correlation between the search cell and its corresponding reference cell; and digital processing circuits for processing said pluralities of correlation sum signal groups and corresponding correlation coordinate signal groups so as to produce weighted correlation coordinate signals (ε_x, ε_y), indicative of the weighted average displacement for the entity of all of the search cell correlation coordinate signals, formed from each cell's displacement, indicative of the position of the subsequent scene in the field of view.

The invention provides a new approach to cross-correlation image matching. This approach employs a multiple sub-area correlation technique in which several sub-areas or cells are selected from the reference image and individually correlated against the sensor image, that is the stored image, creating a set or a plurality of cross-correlation functions.

Preferably there is provided a peak detector circuit responsive to said correlation sum signal groups for producing a correlation peak signal; and circuits including a multiple peak detector for excluding from use in the production of weighted correlation coordinate signals those correlation sum signal groups in which more than one correlation peak is detected.

Advantageously the tracker is a video tracker, including a comparator having a bilevel output which switches between its two output levels each time the signals at its inputs are the same, and circuits for coupling delayed and undelayed video signals, respectively, to different inputs of said comparator so that each time said signals are the same, said comparator switches from one output level to the other.

This generates a single bit digitized video signal without employing a threshold. Hence the digitized video signal is independent of the presence or absence of prominent scene features and is relatively unaffected by changes in brightness or contrast.

A tracker system in accordance with the present invention will now be described by way of example and with reference to the accompanying drawings in which:—

Fig. 1 is a conceptual schematic block diagram of the tracker system;

Fig. 2 is a block diagram of a self thresholding subprocessor for use as element 10 of Fig. 2;

Fig. 3 is a block diagram of an alternative self-thresholding subprocessor for use as element 10 of Fig. 2;

Fig. 4 is a frequency response curve illustrating output amplitudes as a function of frequency for a three pole Bessel roll off filter;

Fig. 5 shows curves representative of input video signal to the video processor of Fig. 2 and output digital video signal from the video processor;

Fig. 6 is a conceptual schematic block diagram of the reference data storage element of Fig. 1;

Fig. 7 is a conceptual schematic block diagram of the live video formatter of Fig. 1;

Fig. 8 is a logic schematic block diagram of the convolver of Fig. 1;

Fig. 9 is a conceptual block diagram of an exemplary master timer as might be used in the tracker system;

Fig. 10 is a block diagram exemplifying externally synchronized tracker operation;

Fig. 11 is a diagram helpful in explaining the operation of the tracker system in which the numbers represent the number of cells with validated correlation peaks at a particular location. (For instance, the number 5 indicates that five cells have unique, validated correlation peaks at location (7, 9).)

Fig. 12 is a diagram helpful in an explanation of the operation of a single correlation cell.

Fig. 13 is an exemplary conceptual diagram of a correlator cell configuration;

Fig. 14 is a timing diagram illustrating the signal output and sequence of events of a master timer as exemplified in Fig. 9;

Fig. 15 is a timing chart showing representative horizontal and vertical blanking and address times as used in the tracker system;

Figs. 16 and 17 are timing charts helpful in an understanding of the sequence of events occurring in the correlator of the tracker system; and

Fig. 18 is a simplified flow chart showing an exemplary mechanization of a stored program for use with the tracker system.

Referring first to Fig. 1, video from a sensor, not shown, enters the video processor 10, a two-level digitized video signal is derived from the video which presents a unique fingerprint for each scene being viewed. Digital video enters the live video formatter 20 which arranges the video signal in a bit stream suitable for sequential real-time processing. Digital video also enters its bit stream or selected portions thereof into the refresh memory and logic 30 where it is buffered for replacing those correlants in the reference data storage memory 40 which were found to provide correlation functions not qualifying in the subsequent validation test. Formatted live data then enter the "N" bit convolver 50 along with the reference data from reference data storage memory 40. The function of the convolver 50 is to determine, and output, the degree of match between live data and reference data, that is, the correlation function. In one preferred embodiment, for example, N equals 64, so that the maximum number of matches is 64. A sum of all matches is computed every 217 nanoseconds, as determined by a master timer (FIG. 9) at a clock rate of 4.6 MHz. The highest value of this sum, as determined by digital peak detector 70, that is, the correlation peak, is stored in the peak magnitude storage 80, together with its coordinates X and Y within its search area. These are placed in the peak coordinate storage 90.

Digital peak detector 70 also provides a search of each search cell for other peaks of either equal level or lower level by a fixed amount. If such ambiguities are present, as shown by multiple peak detector 100, the X, Y data from that particular cell will not be validated and this lack of validation will be stored in the invalid storage latch 110.

The digital data processor 120 performs all computations involving arithmetic, Boolean logic, and decisions. A preferred embodiment uses a programmable central processor unit, operating under command of an instruction set. Other embodiments may be constructed, such as, for example, a hard-wired logic version. The main functions of the digital data processor 120 include the performance of validation tests on all cell correlations by applying criteria which determine a level of confidence, according to peak to side-lobe plus noise, ambiguity, etc.; calculation of the global correlation coordinates from all valid local correlation peak coordinates. (The global correlation coordinates are determined either by simple averaging, first or second moments, or weighted combinations of several of these); control of the updating of correlants (or references) in invalidated cells (this consists of selecting the most likely to match bit stream from the refresh memory, according to the location of well-matching correlants from valid cells); generation of gate coordinates in real time for gate generator 130; and housekeeping and timing functions for the correlator as a whole. Criteria for selection of the reference data are based on a desire for maximum uniqueness or minimum correlation ambiguity when the stored material is correlated against real-time data. Upon switching to a track mode, reference data update ceases, and the most recently stored reference data are frozen in the reference memory 40. Real-time digitized video is clocked through the convolver, in one embodiment, 64 bits at a time; and "Exclusive NOR" comparison is made in the convolver between the stored reference data and the clocked real-time digital video.

Referring still to FIG. 1, the video processor 10 which performs the function of converting raw, unprocessed video to two-level digitized video which has a uniquely coded relationship to the raw video from which it is derived is illustrated. In order to be useful in a correlator, the video processor needs the capability of extracting information from bland, relatively featureless scenes, in which prominent targets or other objects are not necessarily present. Therefore, conventional thresholding techniques which derive a threshold from target amplitude and background measurement and use the derived threshold to digitize a target in the scene are not applicable. In a sense, simple thresholding can be considered to be a form of analog-to-digital conversion with single bit amplitude resolution; if the video signal level is less than the threshold value, the digital video has a value of 0; if the video level is above threshold, digital video has the value 1.

Two configurations of self thresholding video processors are shown in FIGS. 2 and 3. In FIG. 2 a buffer self-thresholding video processor is shown. Composite video on lead 8 is received by buffer 1062. The resulting limited video signal is furnished to bandpass filter 1064 on lead 116. The resulting band limited video is applied to delay network 1066 and comparator 121. Delayed video on lead 119 and undelayed video on lead 118 are applied to comparator 121 whose output is digital video. The digital video output of comparator 121 is furnished to the system on lead 113. A digitized video pattern results over the entire field-of-view, even in the absence of targets or other objects, provided only that scene contrast exceeds sensor coherent noise and random noise.

In the embodiment of FIG. 3, the "zero threshold" processor, the shorted delay line 1072 to ground acts as a quasi differentiator to the bandpassed video. The digital video corresponds to the zero crossings of the bandpassed quasi differentiated video signal.

A bandpass filter 1064 that has been used in the preferred embodiment with a great success is known as a three-pole Bessel bandpass filter. FIG. 4 shows a frequency response curve for such a filter. Raw video from a camera or other sensor passes through a bandpass filter. The filter rolls off at low frequencies in order to attenuate low frequency components associated with sensor shading, scene shading, large-scene features, and sensor microphonic oscillations. As long as the rolloff starts at a frequency above the line-scan frequency (15.75 KHz), its value is not critical. The high frequency cutoff in the filter utilized is approximately 500 KHz. Values of cutoff between 100 KHz and 1 MHz were explored to find an optimum, but it was found that the cutoff frequency was not critical. The high end response is shaped by the Bessel filter chosen for its freedom from preshoot and overshoot and its linear phase response.

Referring to FIG. 5, it is there illustrated how live video may be compared with delayed video in order to develop a digital video signal at the crossings. This technique provides a digitized video signal with a logic 1 and a logic 0 for approximately equal time from bandpassed video of most of the scenes. This is ideal for producing the correlation function, further, this form of digitization is sensitive enough to process very low contrast video almost independent of contrast levels and brightness. Experience with this video processor shows that it is relatively insensitive to scale factor changes in the video. The digital video pattern for a given video scene remains relatively invariant with video amplitude changes down to the level where noise becomes a significant factor.

Referring now to FIG. 6, the reference memory is stored in random access memory devices (RAMS). Any suitable type of memory and storage unit may be utilized such as integrated circuitry, magnetic memory, any dynamic-type memory or any of the other suitable types. The RAMS contain reference data for all of the search cells. The memory is updated by the digital data processor as required by the demand update logic. All the random access memory outputs are inputs to convolver 50.

Referring now to FIG. 7, the live video formatter is illustrated. The convolver receives its live video information from the live video formatter. This live digitized video must be converted from its serial form to a form acceptable by the convolver This is accomplished in the formatter whose block diagram is shown in FIG. 7.

Referring now to FIG. 8, the operation of the convolver will be explained. The mathematical function of the convolver is to compare "live" digitized video (64 binary elements are shown for purposes of illustration) with the reference data (also 64 binary elements), and output a binary number that is the sum of all matches between each of the comparisons. This is done every clock period (in the preferred embodiment, every 216 nano-seconds). Each binary element of live video and its corresponding binary element of reference data are inputs to an Exclusive NOR gate. The output of the Exclusive NOR gate is a logic 1 if the two inputs match and a logic 0 if they don't match. The rest of the convolver determines how many of the 64 Exclusive NORs have a logic 1 output (in the preferred embodiment). This is accomplished by first dividing the Exclusive NOR outputs into eight groups of 8. The eight inputs of each group are then applied to the eight address bits of eight 256 x 4 read-only memories (ROM). Here any suitable type memory device may be utilized such as for example integrated circuitry, magnetic memory, etc. The ROM is programmed so that its output is the sum of 1's on its address. The outputs of the eight ROMs are then summed two at a time with digital adders until the final sum is attained. The digital convolver is capable of very high speed operation. In the preferred embodiment it convolves two 64 element words (real-time live data against stored reference data) and derives a correlation sum (in the preferred embodiment, the sum represents the number of matched elements) every 216 nanoseconds.

In summary, the convolver comprises two basic functional components:

1. "Exclusive NOR" network; these devices detect a match between an element in the reference data word and an element in the live data word. Exclusive OR logic may be used alternatively in order to generate a sum representing the number of mismatches.

2. Convolver summation logic; this logic performs a complete summing operation of matches in each subset of live data compared to the reference data.

During search of a particular live data search cell region by its associated reference, each computation of a new sum (matches) which is larger than all previously determined values during that search, results in a peak detector output which stores the X and Y coordinates of that newest peak value along with the value of correlation match.

A master timer system such as used in the preferred embodiment may be as shown in the block diagram of FIG. 9. 13.8 MHz oscillator 1301 supplies its signal by means of lead 181 to divide-by-3 circuit 1303 which puts out two 4.6 MHz signals by means of leads 183 and 185. Another output of divide-by-3 circuit 1303 is supplied to horizontal counters and decoding system 1305 which also accepts a horizontal preset signal by means of lead 171. Horizontal counters and decoding system 1305 outputs a signal by means of lead 175 to vertical counters and decoding system 1307. Vertical counters and decoding system 1307 receives a vertical preset signal on lead 173. Horizontal counters and decoding system 1305 output horizontal addresses on the lead 177, horizontal timing pulses on lead 161 and a correlator clock signal on lead 163. Vertical counters and decoding system 1307 outputs a vertical address signal on lead 165 and vertical timing pulses on lead 167.

Referring now to FIG. 10, operation of the invention from an arbitrary video source will be explained using a video tape as the arbitrary source. During operation of the invention from a video source such as a video tape recorder 1002, normal synchronization signals are not available. In processing such a signal, the incoming video signal from the video source 1002 is applied to a synchronization signal separator 1004 so as to remove the video content and retain the horizontal and vertical synchronization intelligence. The thus separated horizontal and vertical synchronization signals are applied to gate/correlation tracker 1006 by means of leads 171 and 173 (as shown also in FIG. 9) respectively. Gate/correlation tracker 1006 is also responsive to the original video signal from video source 1002 appearing on lead 1008. The horizontal synchronization signal is applied to the master timer to preset the horizontal rate counters at the beginning of every scan line and vertical synchronization signal is applied to the vertical counters to preset the vertical rate counters at the beginning of every field time. As a result of the foregoing, the video source now generates timing signals which are received by the tracker and thus the tracker synchronizes its own internal timing functions to line up with those of the video source. It has been found necessary to implement such a scheme because so many video sources do not exhibit constant timing signals due to some disablement of the original incoming signal. In the selected case of a video tape, the timing signals occurring with the video signal outputs may not be constant. This inconstancy may be due to wow and flutter or just poor recording or poor quality of the original incoming signal. Since the timing may vary quite a bit, it is necessary to continuously preset the system timing counters on a line-by-line basis and a field-by-field basis to make sure that synchronization with the video source is maintained.

Attention is now directed to FIGS. 11, 12 and 13. The normal analog video signal from a sensor, i.e., TV camera, IR scanner, etc., is first "digitized" by the video processor into a two-level signal called digital video. The scene, that is, the field-of-view, is subdivided into regions or search cells as shown in FIG. 13 (15 cells are shown in this example). The digital video from the center of each region provides the reference which is stored in memory during the last scan prior to initiating the "track" mode. Live video of the subsequent scans in each region is then compared in real time with its corresponding reference. A correlation function is computed for each cell which is a measure of the degree of match (or mismatch) between the reference and live data. Validation criteria are applied to the correlation data to ascertain the usefulness of correlation information derived from the cell. Only displacements derived from validated cells are used for scene position computations. The data from those cells whose correlation function does not meet the requirements of the validation criteria are excluded from further processing. Moreover, the reference data of each invalidated cell are replaced, that is, updated with new digitized video data extracted from that video space which corresponds to the new scene position.

FIG. 12 shows diagrammatically a typical search cell structure with a 64 element reference (four lines of 16 elements each) in the center. In the present embodiment, the reference searches seven lines up, seven lines down, seven elements to the left and seven elements to the right. This means that the search cell comprises an area of eighteen lines (4 + 7 + 7) by 30 (16 + 7 + 7) elements. For this particular implementation, the reference data for all the cells of a line are one continuous segment. Therefore, the horizontal search areas of adjacent cells overlap. FIG. 12 is not strictly in proportion, the hatched overlap areas occupying 28 (14 + 14) elements of the 30 elements in the cell width.

Vertically, the cell search areas are separated by one line. The placement of the cells and their respective overlap depends on the field of view, anticipated zoom rates and types of scenes, etc. As each cell searches seven elements to the left and seven elements to the right, a total of fifteen possible horizontal locations is visited. Likewise in a typical embodiment, there are fifteen possible vertical locations. FIG. 11 shows a matrix of these 225 (15 x 15) possible locations. The "best match" between the reference and live data must occur at one of these 225 locations. If the number of cells having "best matches" at each location is counted and these numbers written in the corresponding squares in FIG. 11, the matrix might appear as shown. This shows a typical correlation peak distribution pattern. Note that the total obtained by adding all the numbers in the squares is the number of valid cells for that scan. In the present embodiment that total can never be higher than 15.

In FIG. 14, square wave illustrations representative of the 13.8 MHz master oscillator A, along with the 4.6 MHz clock signal B, and the 4.6 MHz clock strobe signal C, are shown. These signals appear respectively on leads 181, 185 and 183 of FIG. 9. As shown, the periodicity of the 13.8 MHz signal A is 72 nanoseconds. There is thus as shown a total of 216 nanoseconds between clocks, that is, the rising edges of curve B, representative of the 4.6 MHz clock signal. The purpose of generating the clock strobe signal C and the clock signal B in the manner illustrated is as follows:

On the rising edge of the 4.6 MHz clock (referred to as the clock edge), counters are incremented and necessary functions are initialized as required. As a result of this sharp rise time, it takes a finite time interval for system elements to ripple and settle. A system settling time of 72 nanoseconds is allowed in a system representative of the invention for the purpose of allowing such transients to die down before attempting any data transfers. As shown in waveform C, immediately following the 72 nanosecond system settling time of waveform B, a 72 nanosecond-wide clock strobe signal is initiated. This 72 nanosecond clock strobe allows data transfer according to system requirements during that interval. The sharp fall time of the 72 nanosecond clock signal also causes transients to occur in the system and thus, the trailing edge of this signal is also followed by a system settling waiting time interval of 72 nanoseconds before the occurrence of the next system clock pulse as shown on waveform B. The duration of the clock signal B in this representative system is shown to be 14 nanoseconds while the interval between the pulses of this waveform is shown to be 72 nanoseconds. The duration of the clock strobe is shown to be 72 nanoseconds on waveform C, while the interval between pulses is shown as 144 nanoseconds.

FIG. 15 is helpful in understanding the operation of the horizontal and vertical counters of FIG. 9. As shown, in horizontal blank waveform D, an 11 microsecond pulse is followed by a 52.5 microsecond interval before the occurrence of the next 11 microsecond pulse. The horizontal addresses, comprising a total of 243 addresses, lie in the 52.5 microsecond region as shown. The center position is shown as address 127. The first address is shown as address 126 and the last address is shown as address 248. Thus, horizontal addresses run from 6 through 248 and the center is 6 + 248 = 254 divided by 2 giving 127 as the horizontal address of the center. As indicated, there are 256 correlator clocks which begin slightly prior to and terminate slightly after the 52.5 microsecond period. The available addresses of the 256 correlator clocks are 0 through 255. This implementation is effected because of the existence of system delay lines in the correlator having exactly 256 clock counts applied to them so that there are 256 correlator clocks even though there are only 243 horizontal addresses.

Vertical blanking pulses occur as shown by waveform E and endure for an interval covering exactly 21 lines. Vertical address counters comprise 241 vertical addresses from 7 through 247 and again the center address is 127 so that the exact center of the display is defined as 127 horizontal address and 127 vertical address. In terms of lines, then, a vertical blanking signal of duration 21 lines is followed by an addressing interval of 241.5 lines before the occurrence of the next vertical blanking pulse. There are thus 525 lines per frame comprising 2 x 241.5 = 483 lines, since the display in the representative system is interlaced, plus 2 x 21 = 42 lines of blanking, giving the total of 283 + 42 = 525 lines as in conventional television displays. There are thus 241.5 active lines per field and 21 lines of blanking. However, during this time the system clocks out only 214 addresses since data are not processed on the half line.

The horizontal address counter is an 8-bit counter whose addresses run from address 0 through address 7 while the vertical address counter is also an 8-bit counter whose addresses run from address 0 to address 7. There is thus an 8-bit binary word defining the address of a vertical position and a like word defining the address of a horizontal position, that is, two 8-bit numbers uniquely define an exact point. There exists a total of 241 x 243 = 58,563 possible positions. The correlator, however, only actually searches a total of 225 positions per scan as is indicated by the 15 x 15 matrix of FIG. 11.

In forming a television display in the normal mode of operation of the invention, the tracker master timer sends out horizontal and vertical synchronization pulses to a television camera thus locking the synchronization circuits of the camera to those of the tracker. In conventional television camera equipment, the master oscillator frequency is 31.5 KHz and, therefore, the vertical serration pulse frequency in the system of the invention has been chosen as 31.5 KHz. However, to generate the digital coordinate structure of the system of the invention, a much higher frequency is required. This higher frequency is of the order of 4.6 MHz. The 4.6 MHz frequency is multiplied up by a factor of 3 thus making the highest frequency in the system the 13.8 MHz occurring in the master oscillator of the tracker as shown in FIG. 9. In order to insure maximum system stability, it is only necessary to count down from the 13.8 MHz frequency to the requisite 31.5 KHz frequency and then apply that 13.5 KHz frequency to a conventional television camera to be used with the system. Thus the television camera will be locked to the timing systems of the invention.

Referring to FIGS. 16 and 17, the timing waveforms illustrate the operation of the correlator timing. The number of shift register clocks (SR) required to clock the live data into the shift registers is 16 in this particular configuration. The correlator cell (FIG. 12) is organized as a reference of 16 bits wide by 4 lines high, therefore, 16 shift register clocks are required to load up one set of data horizontally but it is necessary to also have clocked down 4 lines in the vertical dimension in order to be able to perform the first correlation. After clocking down 4 lines, i.e., on the 4th line, and after the 16th clock count, the last piece of data is clocked into the shift register and the system is ready to make the first magnitude measurement. A system delay of one full clock period after the 16th shift register clock allows the correlator to compute the current magnitude. At the end of that delay time period, that magnitude is clocked into a storage latch. The output of the storage latch is them compared to a previously found peak value of magnitude for that cell. It is necessary initially, to set the magnitude of the peak detector equal to zero prior to the first convolution in order to obtain the true peak value for that cell. If the peak detector initially contained any number other than zero, it would be possible subsequently to insert a misleading magnitude into the peak detector. In summary, it is necessary to come down 4 lines of 16 clock counts each. At the end of the 16th clock count, the last piece of data is shifted into the shift register, the system is delayed one full clock time while the convolver computes the first magnitude, and then that magnitude is transferred into the peak detector data storage. On subsequent scans, another piece of data is clocked into the shift register, the oldest piece of data in the shift register just "falls off" the end and is lost, another piece "falls in" and we now have 16 new pieces of data (actually, 15 which were used once before, plus a new one). The next magnitude measurement is now made, and after the one clock period delay, that magnitude is latched and compared to the previously stored peak value. If the latched value is greater, that magnitude is clocked into storage. At the same time that any magnitude is clocked into storage in the peak detector, the coordinates, both X and Y, of that value are also stored with it. Thus, after the system has processed the 225 possible positions for any given cell, there are three numbers for that cell stored in memory. The memory now contains the peak magnitude, which represents the value of the correlation magnitude that was found to be greatest during that search area of 15 positions horizontally on 15 positions vertically, and the X and Y coordinates of where that peak was found to be. After thus processing all 15 cells, there will be stored in memory and accessible by the computer, 15 different magnitudes, and 15 X locations and 15 Y locations, which define where the 15 peaks were found to be. In addition, there are two validation criteria used to determine "good" peaks. First of all, correlation magnitude for a good peak must be above a minimum threshold. That minimum threshold can be controlled by the computer or it can be a dynamic number. In addition, if multiple peaks are found, that is, if there exist two peak values of the same magnitude in a given cell, it cannot be determined which is really the correct one, therefore that cell will be invalidated. Once these 15 peaks have been found, not all of which are necessarily valid, the valid peaks are further processed to compute a "best estimate" of where the scene has moved from the previous scan.

In view of the above, it is evident that for each of the 225 possible positions (FIG. 11) within a given search cell there is a corresponding horizontal address and vertical address set (FIG. 9 and 13) for data applied from the sensor, that is, the correlation sum for a given search cell position is always produced during the time of occurrence of a particular sensor data horizontal and vertical address set. Convolver timing unit 60 of FIG. 1 responds to said sensor horizontal and vertical addresses for providing, in accordance with a fixed, preselected relationship, the cell number and the relative position within the search cell (X and Y location) currently being processed. For example, unit 60 could convert a sensor field address such as line 120 and element 120 (FIG. 13) to a search cell address such as cell 7, position 8, 8 (FIGS. 11 and 13).

Convolver timing unit 60 applies, on a lead 18 (FIG. 1), the cell number to reference data storage unit 40, which unit responds to the cell number so as to provide the proper reference data set to convolver 50, that is the reference data set which is associated with the search cell currently being processed. Similarly, convolver timing unit 60 applies on a lead 56 the cell number to convolver 50 which in turn applies said information in conjunction with the computed correlation sum to digital peak detector 70. Detector 70 uses the cell number information to process the sum correlation information for each of the respective search cells in accordance with the hereinabove outlined criteria; for example, to determine which X, Y position within each search cell has the largest correlation sum. As indicated previously, as each search cell position is processed, the X, Y coordinate information (FIG. 11) associated therewith is applied to peak coordinate storage unit 90 on a lead 26 so that the location within a cell of the correlation peak may be identified; and the cell number is applied on a lead 28 to invalid storage unit 110 so that those cells whose correlation values do not meet preselected criteria may be identified, e.g. two correlation peaks above a given value for a single search cell.

In another tracker system according to the present invention (not shown in the drawings), all the magnitudes for all 15 cells are stored. Thus, 225 magnitudes are stored for each of 15 cells. No validation criteria are performed on these data other than the requirement that it be above a certain minimum magnitude. These magnitudes can run, for example, from 0 to 64 in one embodiment. If, for example, we arbitrarily choose the number 32, any time there is observed a magnitude which is equal to 32 or greater, that value will be stored in memory. The centroid is computed for each cell of the correlation surface that lies above this magnitude, in this case, the number 32. In this implementation, if multiple peaks are found in a cell, it doesn't matter. The centroid is computed for each one of the cells, and the X and Y location for each of the 15 cells along with their centroid computations is used to find out where the scene has moved. A major advantage of using centroid information is, there are more data to work with vis-a-vis one single peak value. It is an integration process that is utilized to generate the centroid. There is thus a tendency to smooth the data, there is lower noise in the output answers than with single points, and greater accuracy is realized. With only one point, resolution is at best to one bit. When a centroid is actually computed, there is a division of a cumulative sum of moments, a moment being defined as the X or Y position multiplied by the magnitude. That sum is divided by the cumulative sum of magnitudes and this then is the centroid. When the division is done, it is unnecessary to stop at merely rounding off to the nearest bit, several bits of sub picture element can actually be maintained. Tests in the lab have demonstrated that this fractional accuracy is valid information. Therefore, instead of only being able to estimate the position of the correlation peak to the closest bit or line (X and Y), it is possible to actually get two or perhaps three bits of sub picture element resolution such that a final answer is obtained by combining the results of all 15 cells. The answer obtained will be better than just within one line or within one picture element, making possible more accurate tracking and also lower noise tracking.

To recapitulate, two methods have been described. There is the peak detection mode where the effort is to find the single peak for a given cell. There may be as many as 15 peaks if all cells are valid. Any cell that has two peak values in different locations will be invalidated. In the second embodiment, single peaks are not evaluated, but all magnitudes which are above some threshold are considered. The centroid of that resulting surface is computed to some sub picture element resolution and this centroid forms the basic data form utilized. The validation criterion used in the embodiment where the centroid computations are performed, is an examination of the total magnitude. Now the total magnitude is the cumulative sum of magnitudes above the threshold. This sum, if found to be greater than some predetermined number, indicates that there exists a reasonably good correlation surface somewhere in that cell.

Referring again to FIGS. 16 and 17, the operation of the timing in an operational embodiment is as follows. After entering the horizontal correlator gate, at the end of the first clock count, there will be one piece of data clocked into the shift register. The process will continue until there is a total of 16 bits of data clocked into the shift register. This is shown as clock 16 on the shift register clock. At the end of this time there are 16 pieces of live data, that have been clocked into the shift register. The convolver now compares that 16 bit grouping to the 16 bits of reference data on that particular line that's stored in reference memory. Since coming down a total of 4 lines, there are 4 lines of data also available. There is a current line and 4 lines of delayed data. That presents a total of 64 possible pieces of data to the convolver. At the end of the 16th clock count of the shift register, the convolver makes its first summation, there is a one full clock period delay, then the result of the magnitude summation is clocked into a latch. There is then a one-third of a clock period delay, or 72 nanoseconds, then these data are strobed into a latch if the magnitude is greater than the stored magnitude, from the peak value of that cell that is being searched. Again, initialization is accomplished by clearing that magnitude of the peak detector at the beginning of the interrogation of every cell so that there is only the peak value of that cell on that particular scan. The drawing also shows a total of 15 possible positions that can be searched for each cell. The addresses can run horizontally from 0 to 14. When address 15 is reached, the write is inhibited, the reference data are changed to the next cell, and on the next clock count the start is at horizontal address 0 again but there is a different cell number. The process is then repeated for each of the cells on that line. The result is that after going through with the horizontal correlator gate, there have been recorded magnitudes for the first vertical search position for five different cells. There are 15 different search positions to be found vertically, thus the system searches a total of 15 positions on each of 15 vertical positions or a total of 225 possible search positions. At the end of the vertical correlator gate all 15 cells have been searched, that is, 225 positions for each of these cells have been searched or interrogated. The system has now either stored the magnitudes, in the case of the embodiment implementing the centroid computation for each of the positions only in magnitudes above threshold, or the peak value for each of the 15 cells has been found, peak value being the magnitude and the X and Y location plus an indication of whether or not the resulting measurement is invalid or valid. If the measurement is invalid that indicates the same peak magnitude occurring twice in a cell on different locations.

When terminal count goes high for the first time inside the correlator gate, then, on the next clock count the horizontal write commands are enabled but thereafter whenever terminal count horizontal goes high the write command is inhibited. The clear is removed from the magnitude latch at the same time terminal count goes high such that on the next clock count the first magnitude can be clocked into the convolver latch. A cell counter enable is provided to increment the counter so as to permit counting from cell zero to cell 1 to cell 2, etc., for the first page, or from cell 5 to cell 6 to cell 7, etc. for the second page, or from cell 10 to cell 11, etc. for the third page. The page counter is used to preset the cell counter such that at the end of the first cell counter enable, during horizontal correlator gate, counting begins from whatever the preset condition was, either 15, 4 or 9. The counter is incremented to give the cell address 0, 5 or 10 depending upon which page is under consideration.

Referring to FIG. 17, the operation in the vertical direction is very similar. The system must process 4 lines before the first magnitude is available, i.e., the first allowable magnitude occurs, at the 4th line. At the 4th line the write is enabled. The write is enabled for a total of 15 different lines, then on the 16th line, which has vertical address 15, the write is inhibited and at the same time the page counter is incremented, so the page counter goes from 0 to 1 to 2, and those values are used to preset the counters to give the correct cell address location for a given page. The latch clear signal is provided in conjunction with the horizontal latch clear signal, also shown on FIG. 16, to prevent the correlation magnitude from being latched into the convolver latch until such time as the system is ready to make magnitude summations. Whenever terminal count 15 occurs vertically, zeros are written to every one of the locations of that group of 5 cells.

FIG. 18 is a simplified flow chart implemented in the preferred embodiment by means of a computer program. Reference to FIG. 18 is now invited for an explanation of the regular routine affected by the central processing unit (CPU).

The program starts out by loading the proper constants into certain operand memory locations. Then since the vertical blank (flag 9) may be in the high state at power turn on, this flag is cleared. Assuming that the correlator is in the "LOAD" mode at power turn on, the correlator gate coordinates are calculated either by assuming that they are centered in the field-of-view if the correlator is working by itself, or slewed to the tracker center lines if the correlator is interfaced with a gated video tracker.

For display purposes, the gate coordinates are loaded to the gate generator only during vertical blanking time. Then the accumulators and scratch pad memories are cleared so as not to interfere with the next field's calculations. After this is done, the CPU is ready for the next field.

At the end of the correlator gate (signified by the energizing of flat 18), all the cells are refreshed automatically from the data in the center of each cell if the correlator is in the "LOAD" mode. This means that the correlator is always loaded with data obtained from the field just before the correlator went into "TRACK".

In the "TRACK" mode, the data that are obtained during gate time are transferred to the CPU after flag 18 occurs. Each cell is then examined for validity by verifying that the correlation peak is above a certain minimum number. Since the multiple peak detection is done in real time, if a multiple peak is detected in a certain cell during gate time, the hardware inputs a number to the CPU that is lower than the minimum acceptable level. This automatically invalidates the cell.

After each cell has been examined for validity, a test is made to verify that there was at least one valid cell during that field. If there are no valid cells, that means that something went drastically wrong. Thus, the reference data are held as is, and the gate position is frozen in hopes that the data will correlate on the next field.

However, in normal operation, most of the cells will be valid. Thus, since it is possible to have 15 different correlation locations, the answers from the valid cells are averaged. This average is used to position the gate over to where the scene has moved, and also to tell the refresh logic from what location to refresh.

During vertical blanking time, the coordinates of the all accumulators and scratch pad memories are cleared.

There has thus been described a scene tracker for use with imaging or quasi-imaging sensors such as television cameras, forward looking infra-red sensors, millimeter wave scanners and the like. It has been shown that the scene tracker of the invention has the capability of extracting information from bland, relatively featureless scenes in which prominent targets are not present. It is thus possible with the invention to perform correlation tracking of scenes with video amplitude variations only slightly larger than the noise level of the system.

Claims

1. A tracker system for scanning a scene in a field of view comprising, a scanner, means (10) responsive to the scanner for producing digital data signals for defining the scene, reference data signal storage means (40) and correlator circuits (20, 50) for comparing reference data signals and live data signals, the latter resulting from a subsequent scan of said scene, and comprising:

circuits (30, 40) for producing search cell data signals from a preselected plurality of portions of the data signals for one scene, and for storing search cell signals from one scan as reference search cell signals;

digital correlation circuits (20, 50) for comparing search cell signals from a subsequent scanning operation with corresponding reference cell signals, on a bit-by-bit basis, and for summing the result of predetermined relationships of said bits, for producing pluralities of correlation sum signal groups, one group for each search and reference cell comparison;

digital coordinate circuits (60) for providing pluralities of correlation coordinate signal groups, one coordinate signal group for each cell, individually indicative of the relative position within each search cell of a correlation between the search cell and its corresponding reference cell; and

digital processing circuits (80, 90, 120) for processing said pluralities of correlation sum signal groups and corresponding correlation coordinate signal groups so as to produce weighted correlation coordinate signals (ε_x, ε_y), indicative of the weighted average displacement for the entity of all of the search cell correlation coordinate signals, formed from each cell's displacement, indicative of the position of the subsequent scene in the field of view.

2. The system of claim 1 characterised by a peak detector circuit (70) responsive to said correlation sum signal groups for producing a correlation peak signal; and

circuits (110, 100) including a multiple peak detector (100) for excluding from use in the production of weighted correlation signals those correlation sum signal groups in which more than one correlation peak is detected.

3. The system of claim 1 characterised in that said tracker is a video tracker, including a comparator (121 or 1070) having a bilevel output which switches between its two output levels

each time the signals at its inputs are the same, and circuits (1066 or 1072) for coupling delayed and undelayed video signals, respectively, to different inputs of said comparator so that each time said signals are the same, said comparator switches from one output level to the other.

Revendications

1. Un système de poursuite destiné à analyser une scène dans un champ comprenant un analyseur, des moyens (10) qui réagissent à l'analyseur en produisant des signaux de données numériques pour définir la scène, des moyens d'enregistrement de signaux de données de référence (40) et des circuits corrélateurs (20, 50) destinés à comparer des signaux de données de référence et des signaux de données courants, ces derniers résultant d'une analyse ultérieure de la scène, et comprenant:

des circuits (30, 40) destinés à produire des signaux de données de cellule d'exploration à partir d'un ensemble présélectionné de parties des signaux de données pour une scène, et à enregistrer des signaux de cellule d'exploration provenant d'une analyse en tant que signaux de cellule d'exploration de référence;

des circuits de corrélation numériques (20, 50) destinés à comparer des signaux de cellule d'exploration provenant d'une opération d'analyse ultérieure avec des signaux de cellule de référence correspondants, en procédant bit à bit, et à faire la somme du résultat de relations prédéterminées de ces bits, afin de produire des ensembles de groupes de signaux de somme de corrélation, avec un groupe pour chaque comparaison de cellules d'exploration et de référence;

des circuits de coordonnées numériques (60) destinés à fournir des ensembles de groupes de signaux de coordonnées de corrélation, avec un groupe de signaux de coordonnées pour chaque cellule, indiquant individuellement la position relative à l'intérieur de chaque cellule d'exploration d'une corrélation entre la cellule d'exploration et sa cellule de référence correspondante; et

des circuits de traitement numériques (80, 90, 120) destinés à traiter les ensembles de groupes de signaux de somme de corrélation et des groupes correspondants de signaux de coordonnées de corrélation de façon à produire des signaux de coordonnées de corrélation pondérés (ε_x, ε_y), représentatifs du déplacement moyen pondéré pour la totalité des signaux de coordonnées de corrélation de cellule d'exploration, formés à partir de chaque déplacement de cellule, et représentatifs de la position de la scène suivante dans le champ.

2. Le système de la revendication 1 caractérisé par un circuit détecteur de pic (70) qui réagit aux groupes de signaux de somme de corrélation en produisant un signal de pic de corrélation; et

des circuits (110, 100) comprenant un détecteur de pics multiples (100) destiné à exclure de l'utilisation dans la génération de signaux de corrélation pondérés les groupes de signaux de somme de corrélation dans lesquels plus d'un pic de corrélation est détecté.

3. Le système de la revendication 1 caractérisé en ce que ce système de poursuite est un système de poursuite vidéo comprenant un comparateur (121 ou 1070) ayant une sortie à deux niveaux qui commute entre ses deux niveaux de sortie chaque fois que les signaux présents sur ses entrées sont les mêmes, et des circuits (1066 ou 1072) destinés à appliquer respectivement des signaux vidéo retardés et non retardés sur des entrées différentes du comparateur, de façon que chaque fois que ces signaux sont les mêmes, le comparateur commute d'un niveau de sortie à l'autre.

Patentansprüche

1. Bildnachführsystem zum Abtasten einer in einem Blickfeld enthaltenen Szene, mit einer Abtasteinrichtung, einer auf die Abtasteinrichtung ansprechenden Einrichtung (10) zur Erzeugung digitaler, die Szene definierender Datensignale, einem Speicher (40) für Bezugsdatensignale und Korrelationsschaltungen (20, 50) zum Vergleich der Bezugsdatensignale mit aktuellen Datensignalen, die von einer nachfolgenden Abtastung der genannten Szene stammen, gekennzeichnet durch

Schaltungsanordnungen (30, 40) zur Erzeugung von Suchzellensignalen aus einer vorgegebenen Anzahl von Abschnitten der einer Szene zugeordneten Datensignale und zum Speichern der Suchzellensignale, die von einer gleichen Abtastung stammen, als Bezugszellensignale,

digitale Korrelationsschaltungen (20, 50) zum Bit-für-Bit-Vergleich von Suchzellensignalen, die von einer nachfolgenden Abtastung stammen, mit entsprechenden Bezugszellensignalen, und zum Summieren des Ergebnisses vorbestimmter Beziehungen zwischen den Bits dieser Signale zur Erzeugung einer Anzahl von Korrelations-Summensignalgruppen, nämlich je einer Gruppe für jeden Vergleich von Suchzellen- und Bezugszellensignalen,

digitale Koordinatenschaltungen (60) zur Erzeugung einer Anzahl von Korrelations-Koordinatensignal gruppen, nämlich je einer Gruppe für jede Zelle, die jeweils den relativen Ort innerhalb einer Suchzelle angibt, an dem eine Korrelation zwischen der Suchzelle und der ihr entsprechenden Bezugszelle vorliegt, und

digitale Verarbeitungsschaltungen (80, 90, 120) zur Verarbeitung der Vielzahl von Korrelations-Summensignalgruppen und der entsprechenden Korrelations-Koordinatensignalgruppen in solcher Weise, daß gewichtete Korrelations-Koordinatensignale (ε_x, ε_y) erzeugt werden, die für die gewichtete mittlere Ver-

schiebung der Gesamtheit der Korrelations-Koordinatensignale, die für die Verschiebung aller Suchzellen gebildet werden, charakteristisch sind und die Position der nachfolgenden Szene im Blickfeld angeben.

2. Bildnachführsystem nach Anspruch 1, gekennzeichnet durch einen Scheitelwertdetektor (70), der auf die Korrelations-Summensignalgruppen anspricht und ein Korrelationsspitzensignal erzeugt, und Schaltungsanordnungen (110, 100) mit einem Mehrfach-Scheitelwertdetektor zum Ausschließen solcher Korrelations-Summen-Signalgruppen von der Verwendung bei der Erzeugung des gewichteten Korrelationsignals, die mehr als eine Korrelationsspitze enthalten.

3. Bildnachführsystem nach Anspruch 1, dadurch gekennzeichnet, daß es sich um ein Video-Nachführsystem handelt, das einen Comparator (121 oder 1070) enthält, der Ausgangssignale mit zwei unterschiedlichen Pegeln liefert und zwischen diesen Pegeln jedesmal umschaltet, wenn die Signale an seinen Eingängen gleich sind, und daß Schaltungsanordnungen (1066 oder 1072) vorhanden sind, die verschiedenen Eingängen des Comparators ein verzögertes bzw. ein unverzögertes Videosignal zuführen, so daß der Comparator immer dann, wenn diese Signale gleich sind, vom einen Ausgangspegel zum anderen umschaltet.

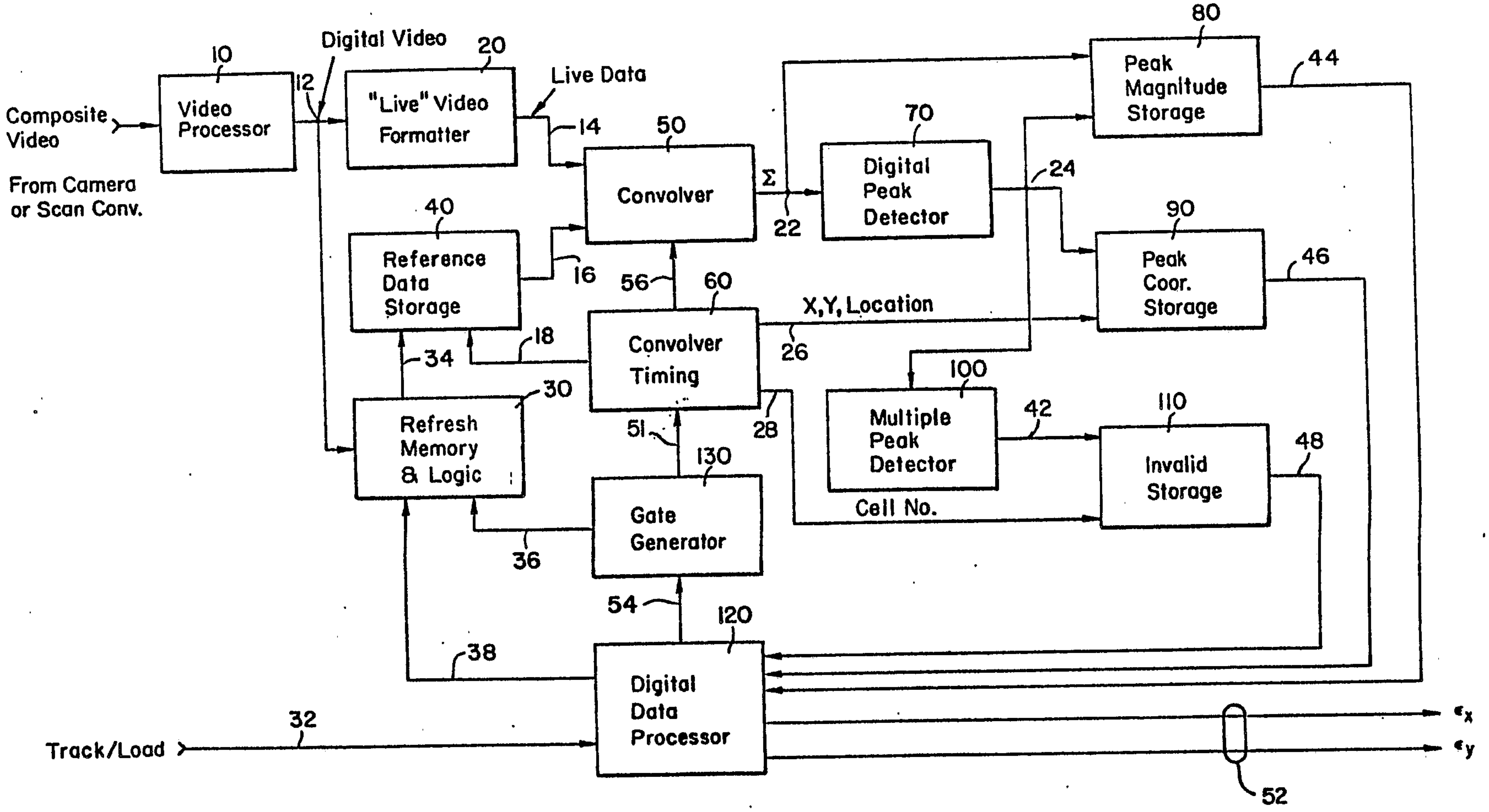

Composite Video
From Camera or Scan Conv.
10
Video Processor
12
Digital Video
20
"Live" Video Formatter
Live Data
14
50
Convolver
Σ
22
70
Digital Peak Detector
24
80
Peak Magnitude Storage
44
40
Reference Data Storage
16
56
60
Convolver Timing
X,Y, Location
26
90
Peak Coor. Storage
46
18
34
30
Refresh Memory & Logic
51
28
100
Multiple Peak Detector
42
110
Invalid Storage
48
Cell No.
130
Gate Generator
36
54
120
Digital Data Processor
38
32
Track/Load
ϵ_x
ϵ_y
52

Fig. 1.

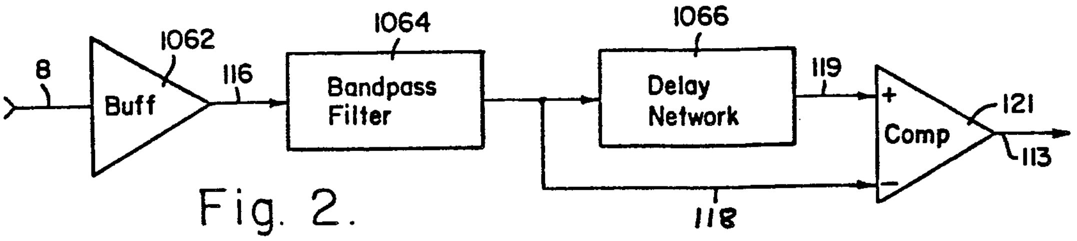


Fig. 2.

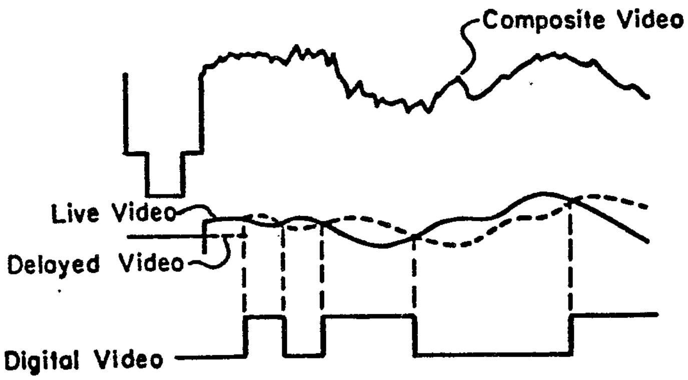


Fig. 5.

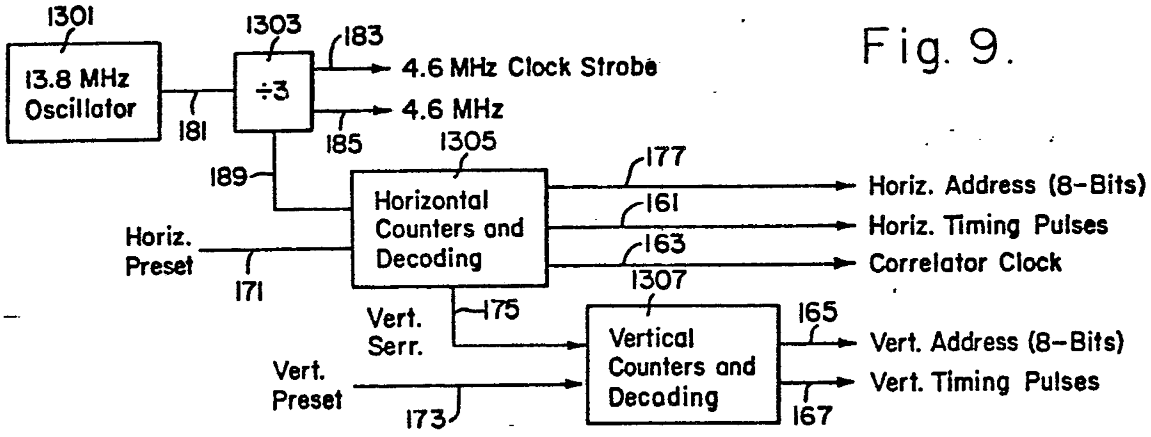


Fig. 9.

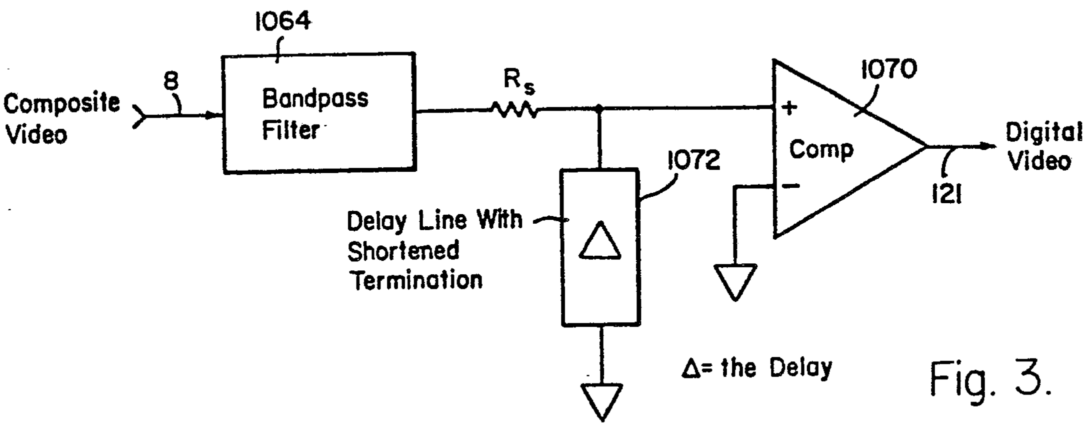


Fig. 3.

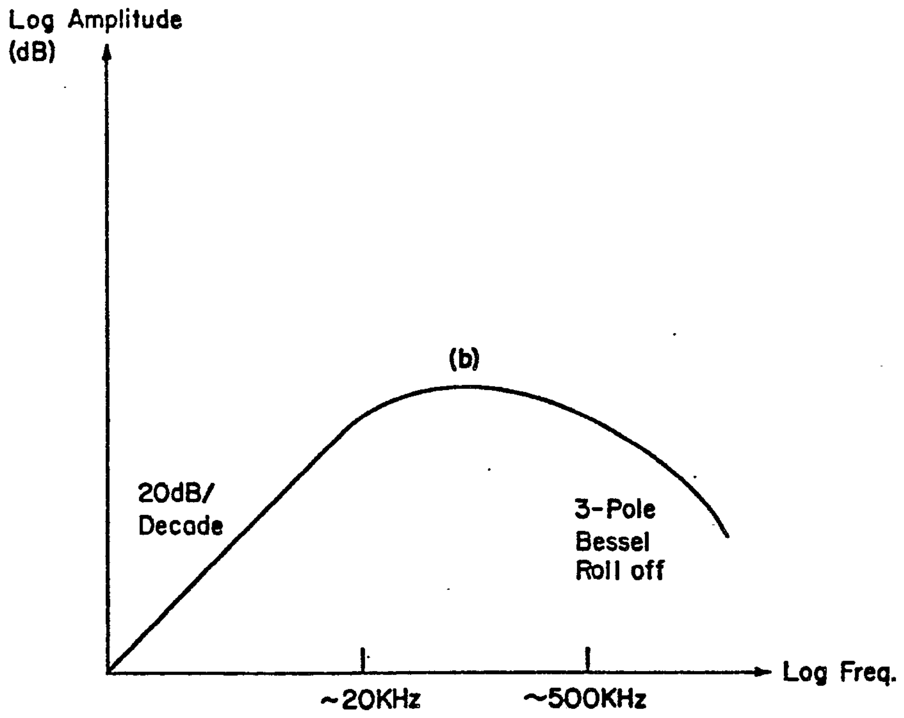

Log Amplitude
(dB)
(b)
20dB/
Decade
3-Pole
Bessel
Roll off
~20KHz
~500KHz
Log Freq.

Fig. 4.

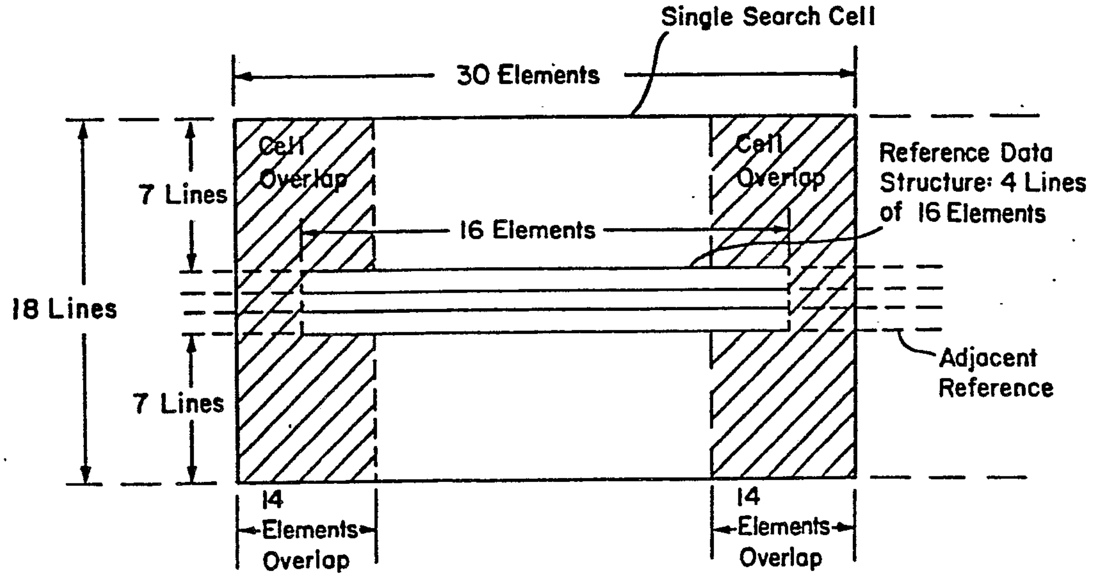

Single Search Cell
30 Elements
Cell
Overlap
Cell
Overlap
Reference Data
Structure: 4 Lines
of 16 Elements
16 Elements
7 Lines
18 Lines
7 Lines
Adjacent
Reference
14
Elements
Overlap
14
Elements
Overlap

Fig. 12.

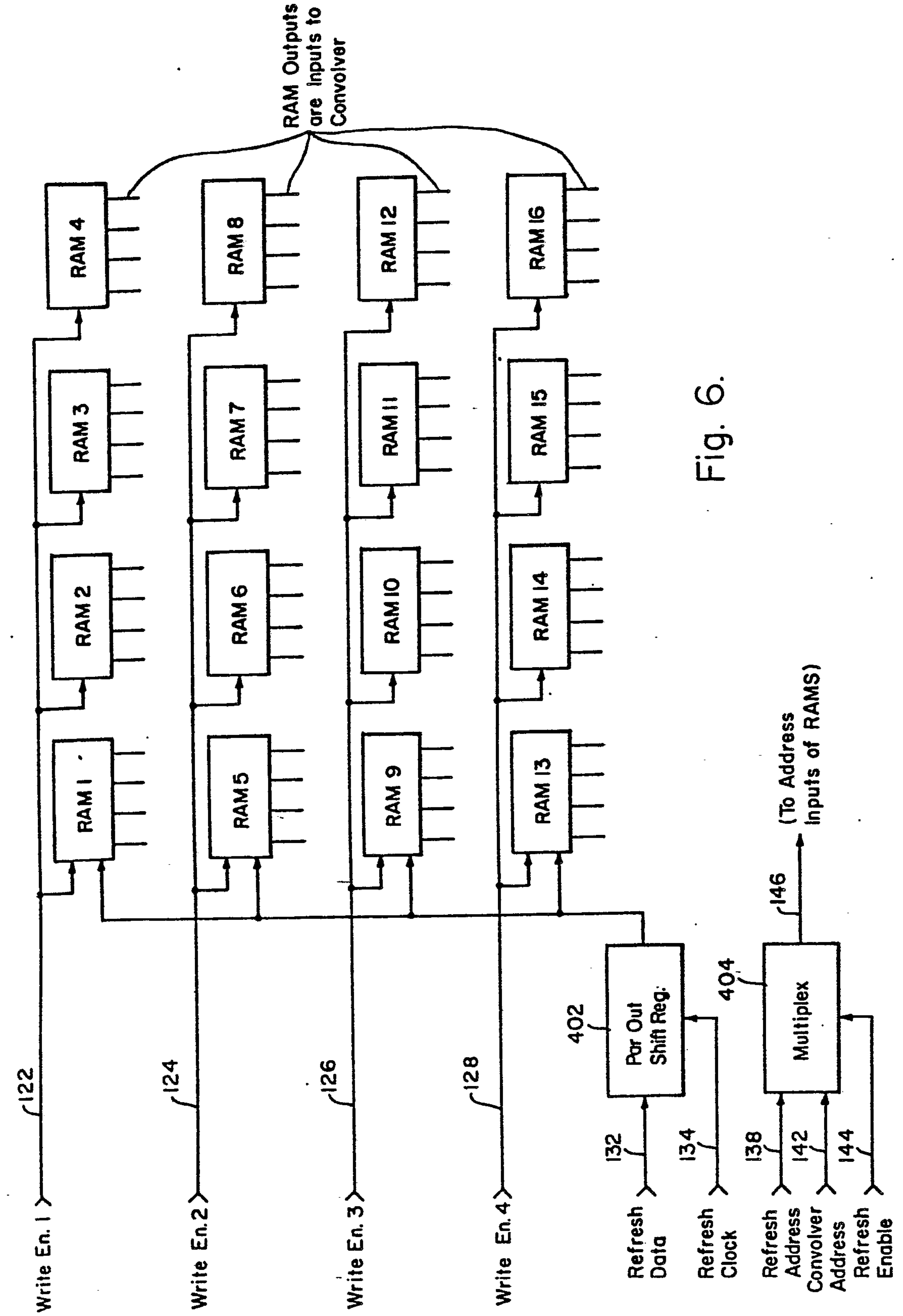

RAM Outputs are Inputs to Convolver
RAM 1
RAM 2
RAM 3
RAM 4
RAM 5
RAM 6
RAM 7
RAM 8
RAM 9
RAM 10
RAM 11
RAM 12
RAM 13
RAM 14
RAM 15
RAM 16
Write En. 1
Write En. 2
Write En. 3
Write En. 4
122
124
126
128
402
Par Out Shift Reg.
404
Multiplex
146
(To Address Inputs of RAMS)
132
134
138
142
144
Refresh Data
Refresh Clock
Refresh Address
Convolver Address
Refresh Enable

Fig. 6.

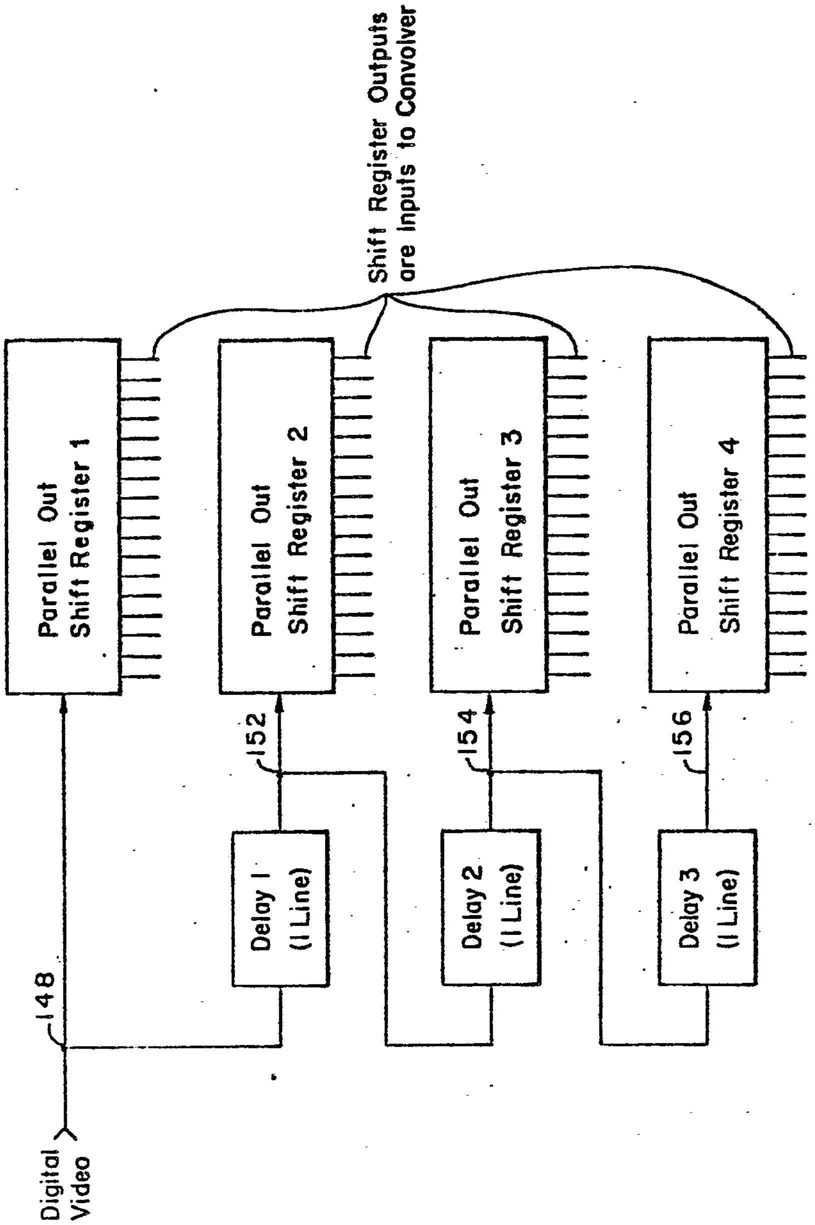

Shift Register Outputs are Inputs to Convolver
Parallel Out Shift Register 1
Parallel Out Shift Register 2
Parallel Out Shift Register 3
Parallel Out Shift Register 4
Delay 1 (1 Line)
Delay 2 (1 Line)
Delay 3 (1 Line)
148
152
154
156
Digital Video

Fig. 7.

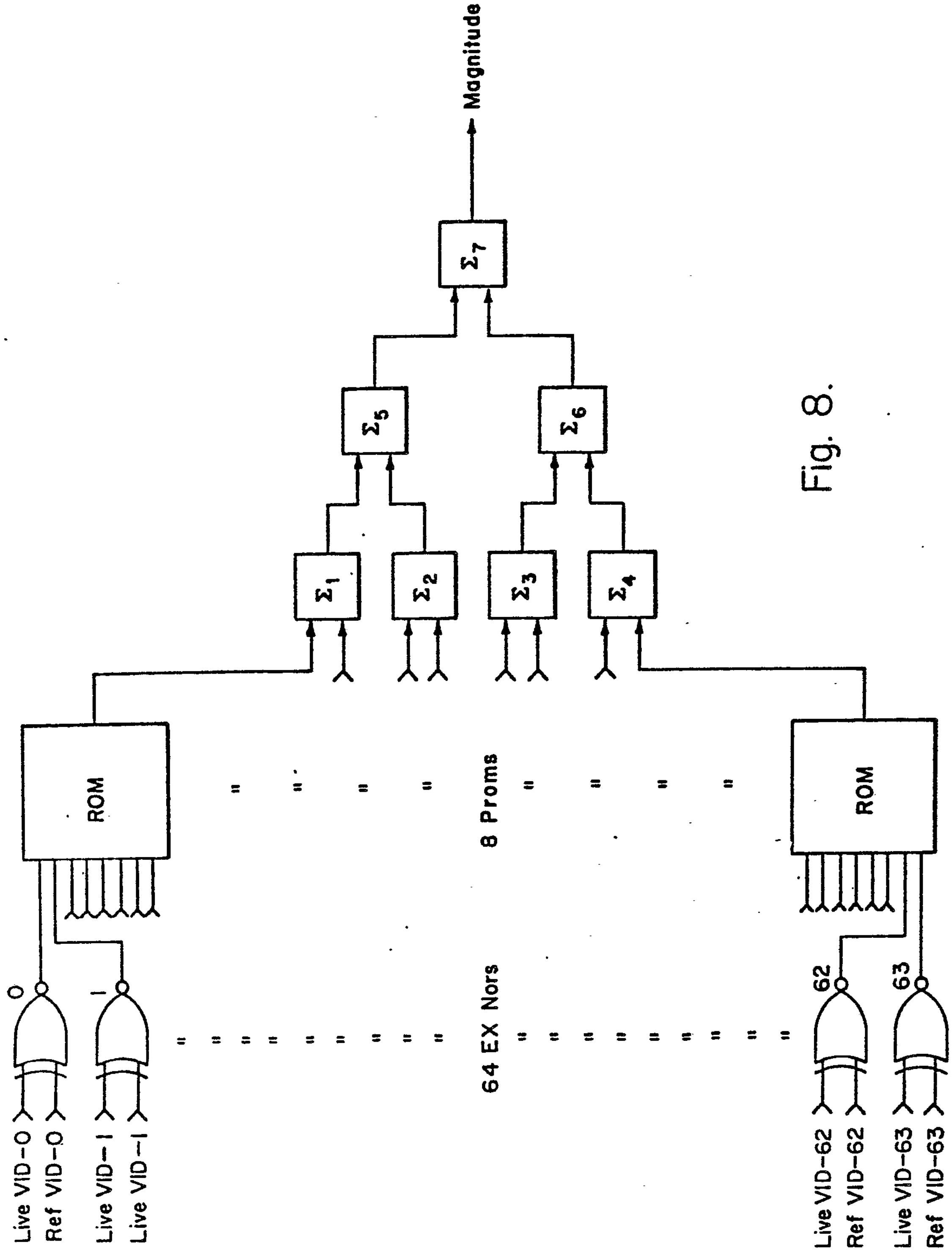

Magnitude
Σ_7
Σ_5
Σ_6
Σ_1
Σ_2
Σ_3
Σ_4
ROM
8 Proms
ROM
0
1
64 EX Nors
62
63
Live VID-0
Ref VID-0
Live VID-1
Live VID-1
Live VID-62
Ref VID-62
Live VID-63
Ref VID-63

Fig. 8.

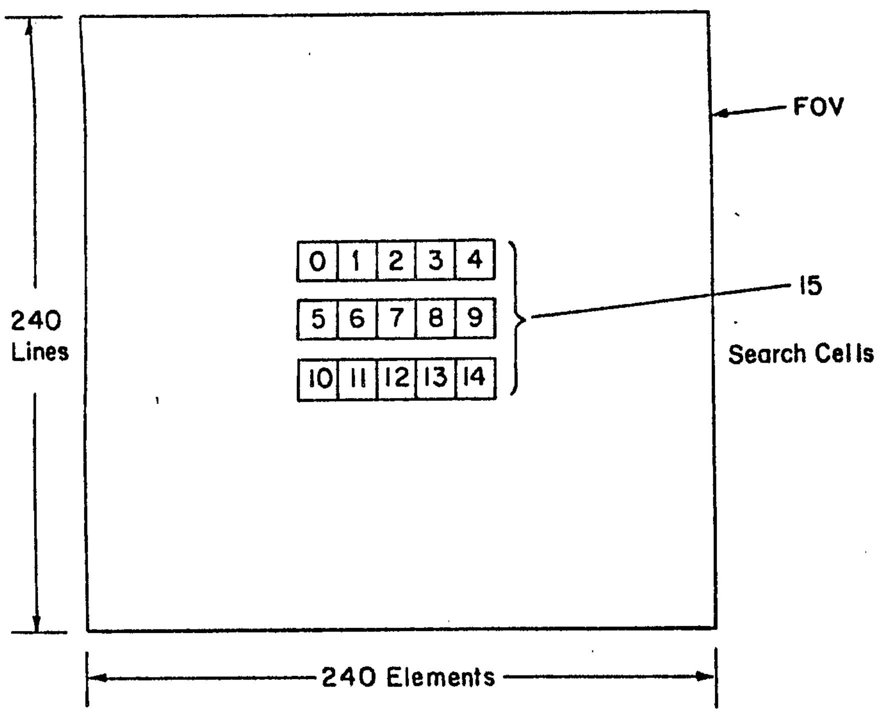


Fig. 13

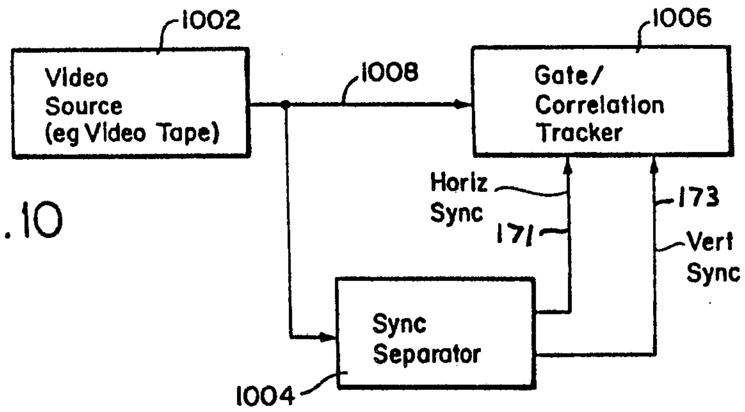
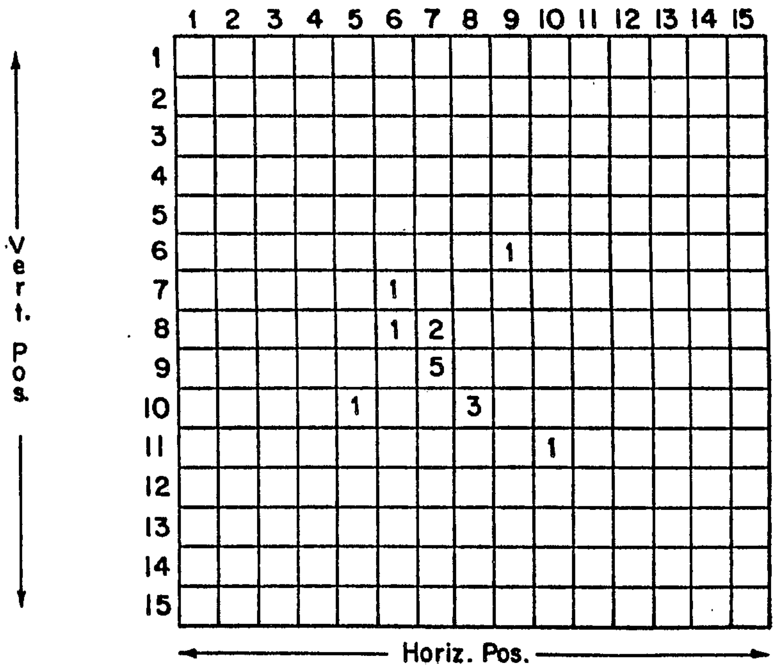


Fig.10



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1															
2															
3															
4															
5															
6									1						
7						1									
8						1	2								
9							5								
10					1			3							
11										1					
12															
13															
14															
15															

Fig. 11.

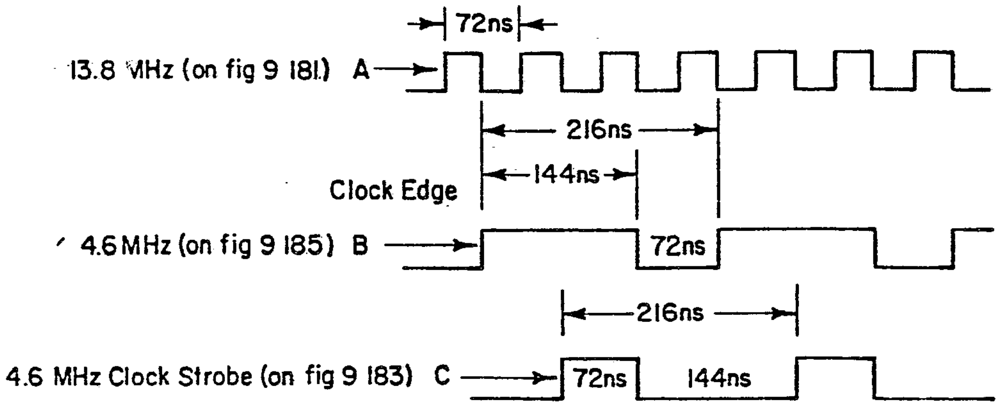

72ns
13.8 MHz (on fig 9 181) A
216ns
Clock Edge
144ns
4.6 MHz (on fig 9 185) B
72ns
216ns
4.6 MHz Clock Strobe (on fig 9 183) C
72ns
144ns

Fig. 14.

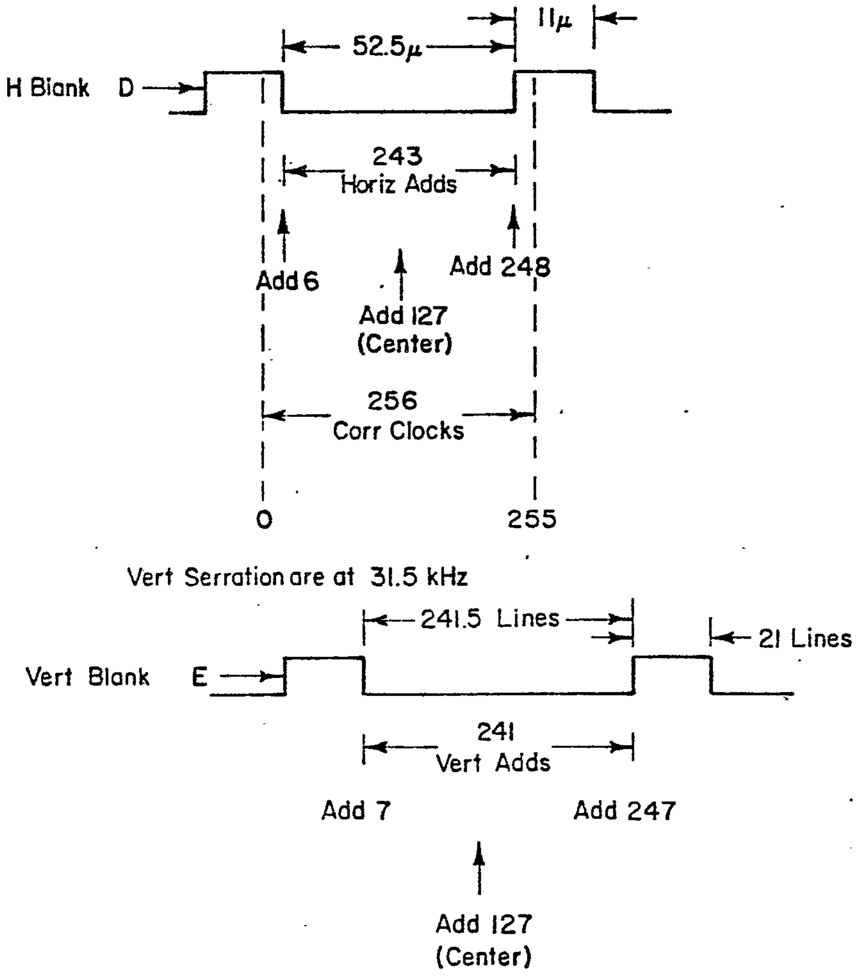

52.5μ
11μ
H Blank D
243
Horiz Adds
Add 6
Add 248
Add 127
(Center)
256
Corr Clocks
0
255
Vert Serration are at 31.5 kHz
241.5 Lines
21 Lines
Vert Blank E
241
Vert Adds
Add 7
Add 247
Add 127
(Center)

Fig. 15.

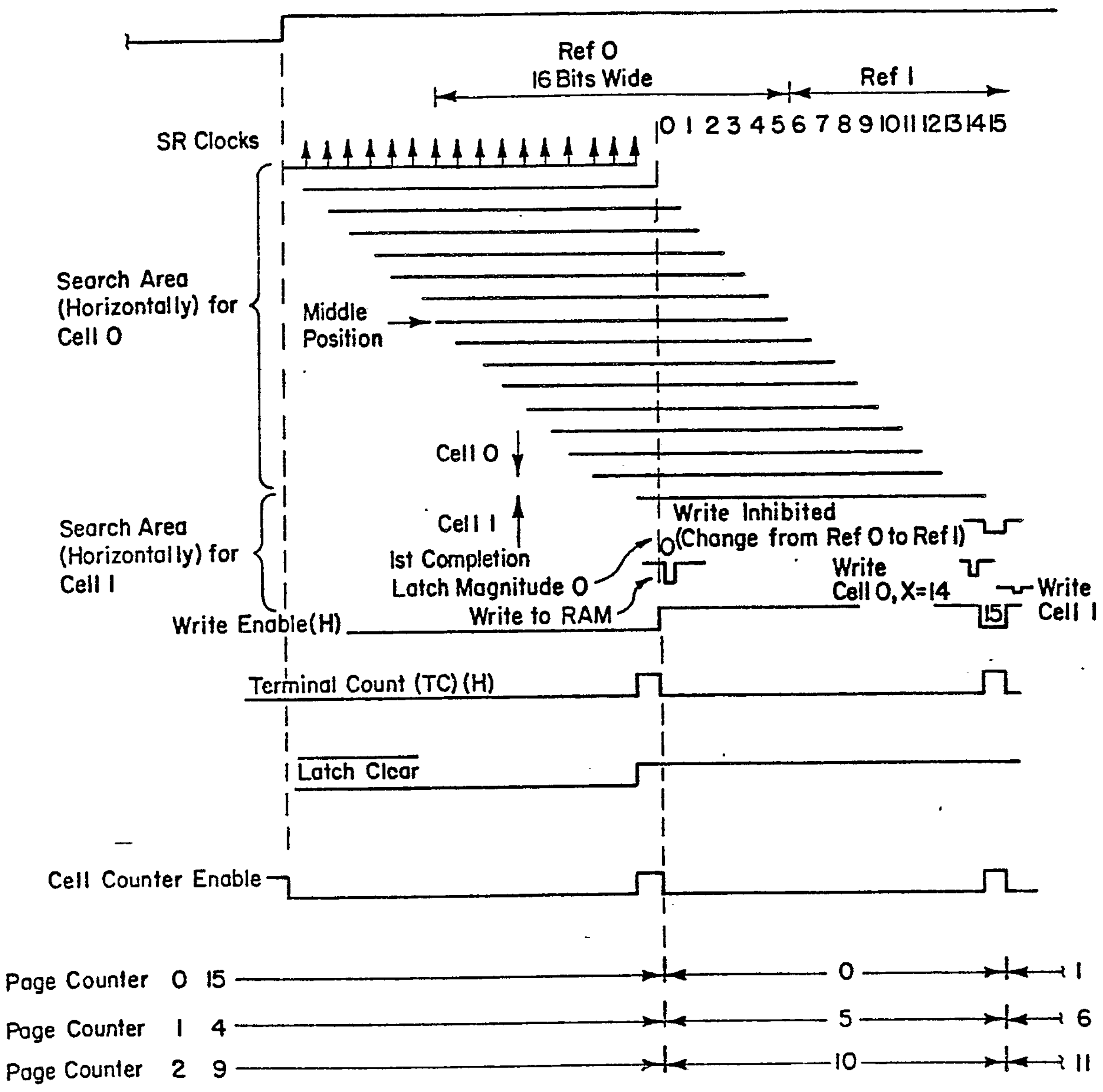

Ref 0
16 Bits Wide
Ref 1
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
SR Clocks
Search Area (Horizontally) for Cell 0
Middle Position
Cell 0
Cell 1
Search Area (Horizontally) for Cell 1
Write Inhibited
0 (Change from Ref 0 to Ref 1)
1st Completion
Latch Magnitude 0
Write to RAM
Write Cell 0, X=14
Write Cell 1
15
Write Enable(H)
Terminal Count (TC) (H)
Latch Clear
Cell Counter Enable
Page Counter 0 15
Page Counter 1 4
Page Counter 2 9
0
1
5
6
10
11

Fig. 16.

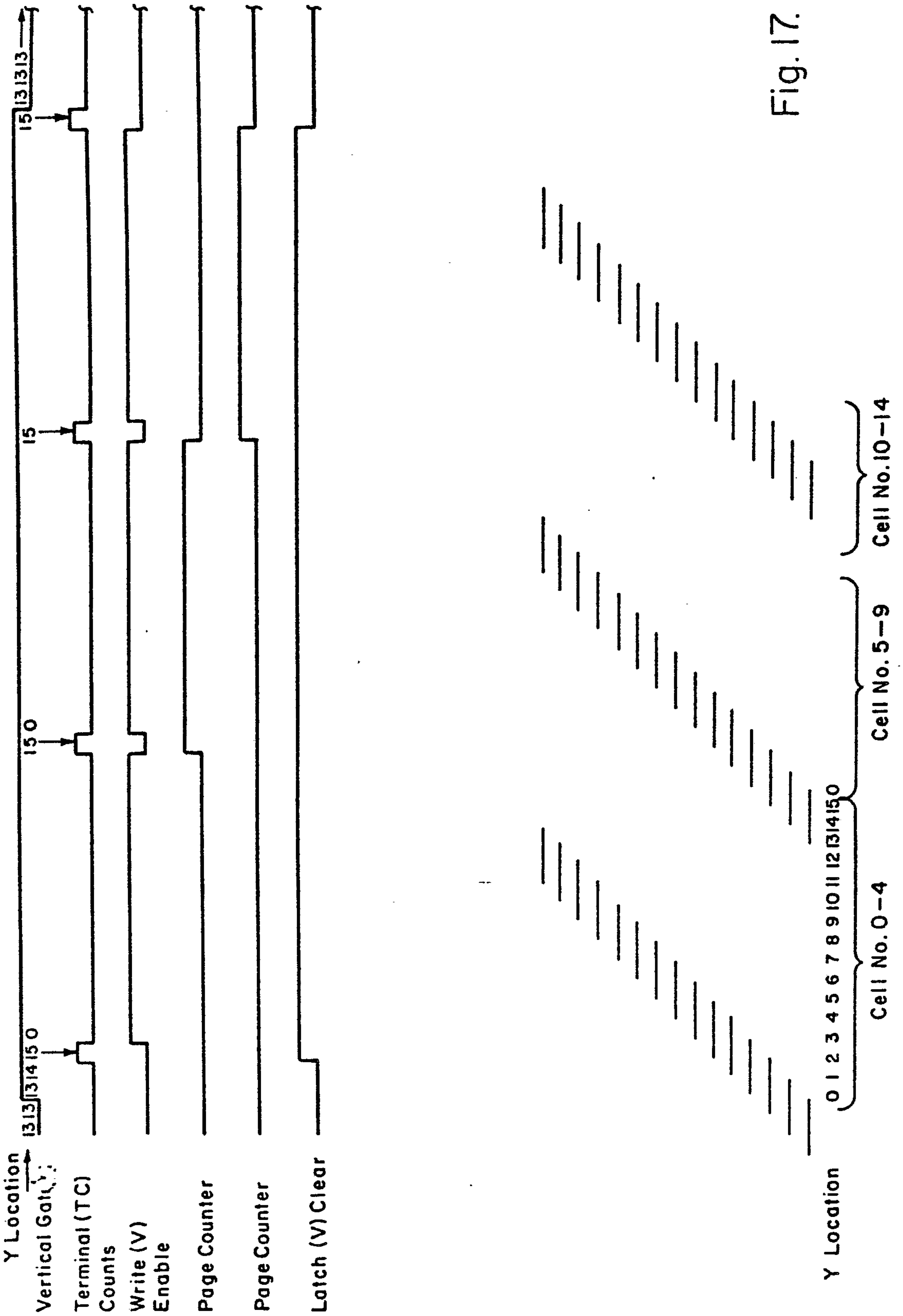

Y Location
Vertical Gate
Terminal (TC) Counts
Write (V) Enable
Page Counter
Page Counter
Latch (V) Clear
13 13 13 14 15 0
15 0
15
15 13 13 13
Y Location
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0
Cell No. 0–4
Cell No. 5–9
Cell No. 10–14

Fig. 17.

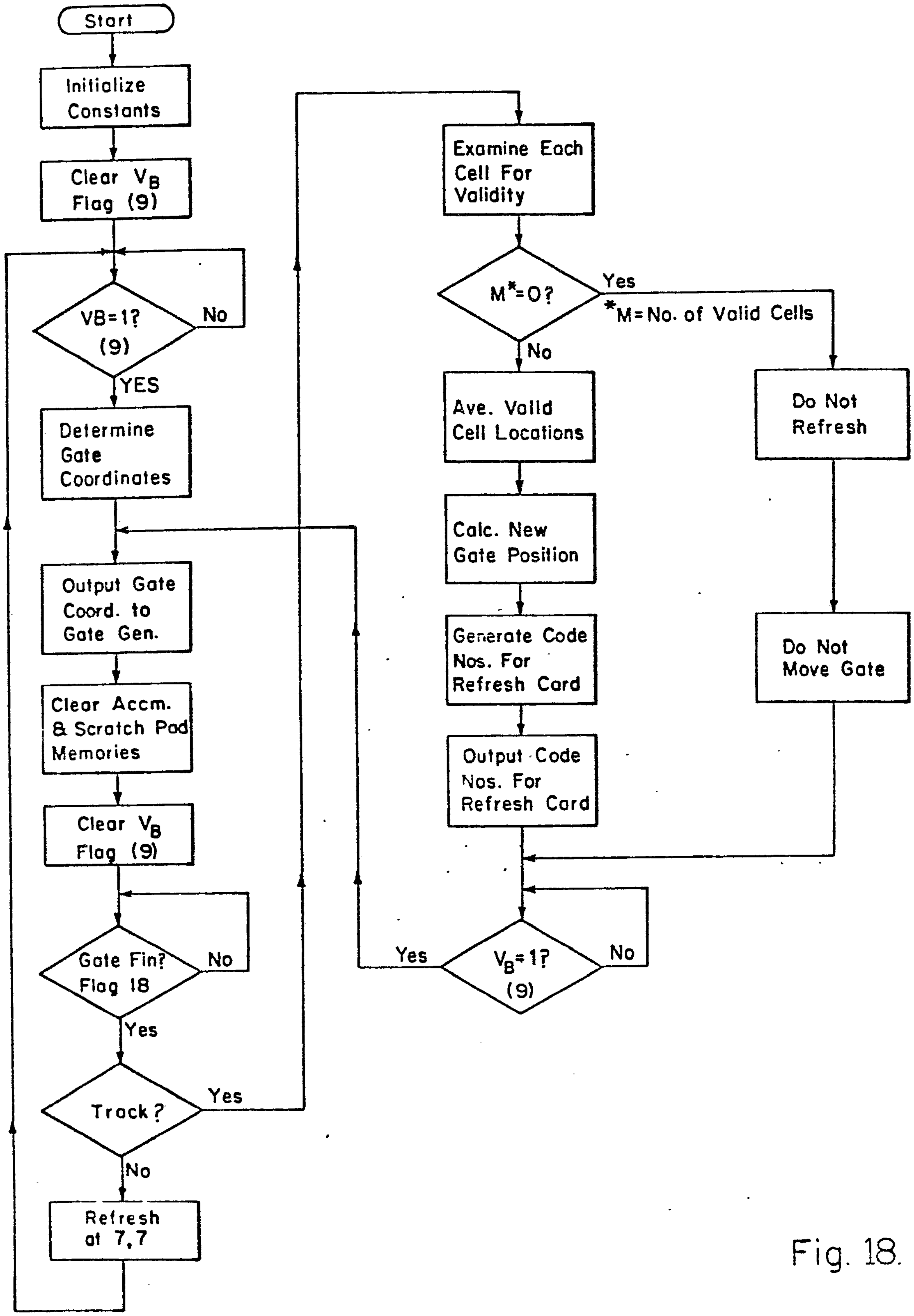

Start
Initialize Constants
Clear V_B Flag (9)
VB=1? (9)
No
YES
Determine Gate Coordinates
Output Gate Coord. to Gate Gen.
Clear Accm. & Scratch Pad Memories
Clear V_B Flag (9)
Gate Fin? Flag 18
No
Yes
Track?
Yes
No
Refresh at 7,7
Examine Each Cell For Validity
M*=0?
Yes
*M=No. of Valid Cells
No
Ave. Valid Cell Locations
Calc. New Gate Position
Generate Code Nos. For Refresh Card
Output Code Nos. For Refresh Card
Do Not Refresh
Do Not Move Gate
V_B=1? (9)
Yes
No

Fig. 18.